



||Jai Sri Gurudev ||

## S J C Institute of Technology, Chickballapur – 562 101

### RESUME

<b>Name</b>	MANJUNATHA Y R			
<b>Date of Birth</b>	15/12/1979			
<b>Address</b>	<p><i>Contact Address: Asst. Professor, Department of ECE, S J C Institute of Technology Chickballapur-562101</i></p> <p><i>Residential Address: Yalagere (Village &amp; Post), Chickballapur (Taluk &amp; District) Karnataka. PIN-562101</i></p> <p><i>Contact Nos: 9845515537</i></p> <p><i>E-mail: manjoo.yr79@gmail.com</i> <span style="float: right;"><i>Mobile:9845515537</i></span></p>			
<b>Department / Discipline</b>				
<b>Educational Qualifications</b>	<b>Exam Passed</b>	<b>Institution   University</b>	<b>% &amp; Class Obtained</b>	<b>Year</b>
	PG: M.Tech	S J C Institute of Technology, VTU	68.5%, First	2005
<b>Experience</b>	<b>Nature of Experience</b>		<b>No. of Years</b>	
	Teaching		16	
	Industry/Research		-	
	Total No. of years of Experience		16	
<b>Experience Details</b>	<b>Designation</b>	<b>Institution/ Organization</b>	<b>Duration</b>	
	Lecturer	S J C Institute of Technology	2005-2010 / 5 Years	
	Senior Lecturer	S J C Institute of Technology	2010-2011 / 1 Year	
	Asst. Professor	S J C Institute of Technology	2011-Till Date / 10 Years	
<b>Professional bodies Membership details</b>	<ul style="list-style-type: none"> <li>Life Member of the IETE: AM-21062</li> <li>Member Institute of Engineers: M-154257-5</li> </ul>			
<b>Areas of Research Interest &amp; Guidance</b>	<ul style="list-style-type: none"> <li>Digital system design using Verilog &amp; VHDL, VLSI &amp; Embedded system design, Image Processing</li> <li>Guided 13+ PG projects and 25+ UG projects</li> <li>Guided 1 KSCST sponsored Project</li> </ul>			
<b>Distinctions/Awards Received</b>	<ul style="list-style-type: none"> <li>Certificate of Achievement-“Quality management System-Internal Auditor Training Course”</li> <li>Best guide award towards motivating and encouraging the students to present the innovative papers at IET'17</li> </ul>			
<b>National/ International Work Shops/ Seminars / Conferences Attended</b>	<ul style="list-style-type: none"> <li>Attended 35+ FDPs/ Workshops / Conferences/webinars/ Seminars</li> <li>Organized one International Conference</li> <li>Organized 6+ FDPs/ Workshops / Conferences/webinars/ Seminars</li> <li></li> </ul>			
<b>No. of Papers Presented/ Books Published</b>	<ul style="list-style-type: none"> <li>Published 2 papers in indexed journals</li> <li>Published 3 papers in other journals</li> <li>Published 1+ conference proceedings</li> <li>Presented 2 Papers in International Conferences</li> </ul>			
<b>NPTEL/ Refresher courses Completed</b>	<ul style="list-style-type: none"> <li>Completed 3 NPTEL Courses and 1 Refresher course</li> </ul>			
<b>Delivery of Invited Talks / Speech at Seminars / Workshops</b>	<ul style="list-style-type: none"> <li>Delivered 4 Invited talks</li> </ul>			

**Significant Contributions**

- Completed / Ongoing funded projects
- ✓ 14.3 Lakhs from AICTE under MODROB Scheme for the modernization of VLSI Lab during 1995-96
- ✓ 6.76 Lakhs from AICTE under MODROB Scheme for the modernization of HDL Lab during 2019-21
- 10+ Consultancy works carried out